COURSE DESCRIPTION CARD - SYLLABUS

Course name

PO 2.4.2 Zaawansowane projektowanie systemów FPGA - EC 2.4.2 Advanced FPGA system design

Course

Field of study
Teleinformatics

Year/Semester
1/2

Area of study (specialization)

Profile of study
general academic

Level of study
second-cycle studies

Course offered in
Polish

Form of study
full-time

Requirements
elective

Number of hours

Lecture
30

Laboratory classes
30

Other (e.g. online)

Tutorials
0

Projects/seminars
0/0

Number of credit points

4

Lecturers

Responsible for the course/lecturer:
dr inż. Łukasz Matuszewski

Responsible for the course/lecturer:
dr inż. Michał Maćkowski

Prerequisites

Knows the analysis and synthesis of digital combinational and sequential circuits, understands the basic digital functional blocks, the principles of designing complex digital courses, and their implementation. Has knowledge of the structure and operation of ICT systems with the use of digital systems.

Course objective

1. Provide students with advanced knowledge in designing digital circuits for programmable circuits.
2. Developing students' skills in solving complex design and implementation problems related to programmable systems.
3. Shaping and developing students' skills of acquiring knowledge about current solutions used in programmable systems.

Course-related learning outcomes

Knowledge

Knows modern advanced tools for simulating the operation of FPGAs. Knows advanced high-level hardware description languages. Has an insightful knowledge of FPGAs' structure and design methods such as serial, parallel, and pipeline implementations used in microprocessor systems.

Skills

Can design and implement a hardware module in the FPGA technique. Knows modern advanced tools for simulating the operation of FPGAs. Knows advanced high-level hardware description languages. Has an insightful understanding of FPGAs' structure and design methods, such as serial, parallel, and pipeline implementations used in microprocessor systems. Can use high-level hardware description languages to implement hardware modules with microprocessor systems. Can perform simulation analysis of digital circuits (including FPGA) using simulation tools and identify signals that students should monitor. In the literature and on the Internet, you can find information on the implementation of projects in the FPGA technique. He can present the created project in FPGA technique and present its good and bad sides. Can use high-level hardware description languages to implement IP core hardware modules and communication interfaces between them.

Social competences

Is aware of other high-level hardware description languages. Understands that designing hardware circuits takes place in large teams where it is necessary to apply design and testing rules.

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

In the field of lectures, verification of the assumed learning outcomes is carried out by assessing the knowledge demonstrated in the exam. The exam is about answering questions and solving problems. To get a grade of 3.0, it is necessary to get a minimum of 50% of the points; 3.5 - 60% of points; 4.0 - 70% of points; 4.5 - 80% of points; 5.0 - 90% points.

A grading scale was adopted: very good (A) - 5.0; good plus (B) - 4.5; good (C) - 4.0; sufficient plus (D) - 3.5; satisfactory (E) - 3.0; insufficient (F) - 2.0

Summative assessment in the field of laboratory exercises - verification of the assumed learning outcomes is carried out by: • substantive assessment of the performance of laboratory tasks - 15 points, • continuous assessment during each class (oral answers) - 5 points, • grades obtained during written tests - 5 points, • obtaining additional points for activity during classes - 5 points.

To get a grade of 3.0, it is necessary to get a minimum of 50% of the points; 3.5 - 60% of points; 4.0 - 70% of points; 4.5 - 80% of points; 5.0 - 90% points.

A grading scale was adopted: very good (A) - 5.0; good plus (B) - 4.5; good (C) - 4.0; sufficient plus (D) - 3.5; satisfactory (E) - 3.0; insufficient (F) - 2.0

Programme content

Lecture:
1. Alignment of essential knowledge for the Verilog hardware description language.
2. Presentation of advanced features of the System Verilog language and BlueSpec elements.
3. To introduce the System C hardware description language.
4. Presentation of hardware description libraries based on Python: MyHDL and MiGen.
5. The problem of constructing Fault-tolerant systems.
6. Designing circuits in the BIST (Built-in Self Test) methodology.
7. Presentation of the JTAG interface.

Laboratory exercises:
1. Using the knowledge gained during the lecture to design and implement hardware modules.
2. Using the BIST methodology for circuit testing.
3. Acquainting the practical use of the JTAG interface.

Teaching methods

Lecture: multimedia presentation with examples presented on the blackboard.
Laboratories: Multimedia show, implementation of laboratory exercises according to the instructions, independent task solving. Work on computers with dedicated software and didactic kits for testing implemented FPGAs.

Bibliography

Basic

- S. Palnitkar, Verilog HDL (2nd Edition), Prentice Hall Professional, 3 mar 2003.
- M. Pawłowski, A. Skorupski, Projektowanie złożonych układów cyfrowych, WKiŁ, 2010.
- M. Węgrzyn, A. Barkalov, Design of Control Units with Programmable Logic. Zielona Góra 2006.

Additional

- J. Bieganowski, G. Wawrzyniak, Jezyk Verilog w projektowaniu układów FPGA.
- R. Woods, J. McAllister, Yi Y. Lightbody, FPGA-based Implementation of Signal Processing Systems,Wiley,2008.
- S. Kilts, Advanced FPGA DESIGN, Wiley 2007.

Breakdown of average student's workload

	Hours	ECTS
Total workload	120	4.0
Classes requiring direct contact with the teacher	64	3.0
Student's own work (preparation for tests, preparation for laboratory classes, preparation for exam, literature studies)	56	1.0